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		Application Number	10/824/132		
		Filing Date	04/14/2004		
		First Named Inventor	Yi-Nien Su et al.		
		Art Unit	2891		
		Examiner Name	Victor V. Yevsikov		
Sheet		of		Attorney Docket Number	N1085-00265

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
VY		A. KAJITA, et al., Highly Reliable Cu/low-k Dual-Damascene Interconnect Technology with Hybrid (PAE/SiOC) Dielectrics for 65 nm-node High Performance eDRAM, Proceedings of the IEEE 2003 International Interconnect Technology Conference, June 2003	

Examiner Signature	V. Yevsikov	Date Considered	09/22/05
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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